What is claimed is:

1. A method for the creation of a seal ring over a semiconductor device, comprising:

providing a substrate, said substrate having been provided with semiconductor devices;

patterning in a layer of dielectric deposited over the substrate first device features having a width dimension concurrent with patterning second device features having a diameter dimension, the width dimension being smaller than the diameter dimension.

2. The method of claim 1, the first device features comprising a device seal ring.

3. The method of claim 1, the second device features comprising via openings.

4. The method of claim 1, the second device features comprising at least one Alignment Mark.

5. The method of claim 1, the width dimension being about 0.15 μm.

6. The method of claim 1, the diameter dimension being about 0.20 μm.

7. A method for the creation of a seal ring over a semiconductor device, comprising:

providing a substrate, said substrate having been provided with semiconductor devices; and

concurrently patterning a seal ring having a width dimension and via openings having a diameter dimension in a layer of dielectric deposited over the substrate, the width dimension and the diameter dimension being mutually dependent.

8. The method of claim 7, the width dimensions being smaller than the diameter dimensions.

9. The method of claim 7, the width dimension being about 0.15 μm.

10. The method of claim 7, the diameter dimension being about 0.20 μm.

11. A method for the creation of a seal ring over a semiconductor device, comprising:

providing a substrate, said substrate having been provided with semiconductor devices; and

concurrently patterning a seal ring having a width dimension and via openings having a diameter dimension in a layer of dielectric deposited over the substrate, the width dimensions being about 0.15 μm, the diameter dimension being about 0.20 μm.

12. A method for the creation of a seal ring over a semiconductor device, comprising:

providing a substrate, said substrate having been provided with semiconductor devices; and

concurrently patterning a seal ring having a first Critical Dimension and at least one Alignment Mark having a second Critical Dimension in a layer of dielectric deposited over the substrate, the first Critical Dimension and the second Critical Dimension being mutually dependent.

13. The method of claim 12, the first Critical Dimension being smaller than the second Critical Dimension.

14. The method of claim 12, the first Critical Dimension being about 0.15 μm.

15. The method of claim 12, the second Critical Dimension being about 0.20 μm.

16. A method for the creation of a seal ring over a semiconductor device, comprising:

providing a substrate, said substrate having been provided with semiconductor devices; and

concurrently patterning a seal ring having a first Critical Dimension and at least one alignment Mark having a second Critical Dimension in a layer of dielectric deposited over the substrate, the first Critical Dimension being smaller than the second Critical Dimension.

17. The method of claim 16, the first Critical Dimension being about 0.15 μm.

18. The method of claim 16, the second Critical Dimension being about 0.20 μm.

19. A method for the creation of a seal ring over a semiconductor device, comprising:

providing a substrate, said substrate having been provided with semiconductor devices; and

concurrently patterning a seal ring having a first Critical Dimension and at least one via opening having a second Critical Dimension and at least one Alignment Mark having a third Critical Dimension in a layer of dielectric deposited over the substrate, the first Critical Dimension and the second Critical Dimension the third Critical Dimension being mutually dependent.

20. The method of claim 19, the first Critical Dimension being smaller than the second Critical Dimension and the third Critical Dimension.

21. The method of claim 19, the first Critical Dimension being about 0.15 μm.

22. The method of claim 19, the second Critical Dimension being about 0.20 μm.

23. The method of claim 19, the third Critical Dimension being about 0.20 μm.

24. A method for the creation of a seal ring over a semiconductor device, comprising:

providing a substrate, said substrate having been provided with semiconductor devices; and

concurrently patterning a seal ring having a first Critical Dimension and at least one via opening having a second Critical Dimension and at least one Alignment Mark having a third Critical Dimension in a layer of dielectric deposited over the substrate, the first Critical Dimension being smaller than the second Critical Dimension and the third Critical Dimension.

25. The method of claim 24, the first Critical Dimension being about 0.15 μm.

26. The method of claim 24, the second Critical Dimension being about 0.20 μm.

27. The structure of a seal ring over a semiconductor device, comprising:

a substrate, said substrate having been provided with semiconductor devices;

in a layer of dielectric deposited over the substrate, a pattern of first device features having a width dimension and a pattern of second device features having a diameter dimension, the width dimension being smaller than the diameter dimension.

28. The structure of claim 27, the first device features comprising a device seal ring.

29. The structure of claim 27, the second device features comprising via openings.

30. The structure of claim 27, the second device features comprising at least one Alignment Mark.

31. The structure of claim 27, the width dimension being about 0.15 μm.

32. The structure of claim 27, the diameter dimension being about 0.20 μm.

33. A structure of a seal ring over a semiconductor device, comprising:

a substrate, said substrate having been provided with semiconductor devices; and

a seal ring having a width dimension and via openings having a diameter dimension having been patterned in a layer of dielectric deposited over the substrate, the width dimension and the diameter dimension being mutually dependent.

34. A structure of claim 33, the width dimensions being smaller than the diameter dimensions.

35. A structure of claim 33, the width dimension being about 0.15 μm.

36. A structure of claim 33, the diameter dimension being about 0.20 μm.

37. A structure of a seal ring over a semiconductor device, comprising:

a substrate, said substrate having been provided with semiconductor devices; and

a seal ring having a width dimension and via openings having a diameter dimension having been patterned in a layer of dielectric deposited over the substrate, the width dimensions being about 0.15 μm, the diameter dimension being about 0.20 μm.

38. A structure of a seal ring over a semiconductor device, comprising:

a substrate, said substrate having been provided with semiconductor devices; and

a seal ring having a first Critical Dimension and at least one Alignment Mark having a second Critical Dimension having been patterned in a layer of dielectric deposited over the substrate, the first Critical Dimension and the second Critical Dimension being mutually dependent.

39. The structure of claim 38, the first Critical Dimension being smaller than the second Critical Dimension.

40. The structure of claim 38, the first Critical Dimension being about 0.15 μm.

41. The structure of claim 38, the second Critical Dimension being about 0.20 μm.

42. A structure of a seal ring over a semiconductor device, comprising:

providing a substrate, said substrate having been provided with semiconductor devices; and

concurrently patterning a seal ring having a first Critical Dimension and at least one alignment Mark having a second Critical Dimension in a layer of dielectric deposited over the substrate, the first Critical Dimension being smaller than the second Critical Dimension.

43. The structure of claim 42, the first Critical Dimension being about 0.15 μm.

44. The structure of claim 42, the second Critical Dimension being about 0.20 μm.

45. A structure of a seal ring over a semiconductor device, comprising:

a substrate, said substrate having been provided with semiconductor devices; and

a seal ring having a first Critical Dimension and at least one via opening having a second Critical Dimension and at least one Alignment Mark having a third Critical Dimension having been patterned in a layer of dielectric deposited over the substrate, the first Critical Dimension and the second Critical Dimension the third Critical Dimension being mutually dependent.

46. The structure of claim 45, the first Critical Dimension being smaller than the second Critical Dimension and the third Critical Dimension.

47. The structure of claim 45, the first Critical Dimension being about 0.15 μm.

48. The structure of claim 45, the second Critical Dimension being about 0.20 μm.

49. The structure of claim 45, the third Critical Dimension being about 0.20 μm.

50. A structure of a seal ring over a semiconductor device, comprising:

a substrate, said substrate having been provided with semiconductor devices; and

a seal ring having a first Critical Dimension and at least one via opening having a second Critical Dimension and at least one Alignment Mark having a third Critical Dimension having been patterned in a layer of dielectric deposited over the substrate, the first Critical Dimension being smaller than the second Critical Dimension and the third Critical Dimension.

51. The structure of claim 50, the first Critical Dimension being about 0.15 μm.

52. The structure of claim 50, the second Critical Dimension being about 0.20 μm.